In the Claims

Amend claims 1 and 10 as follows:

1. (Currently Amended) A method for parametric testing integrated circuit packages having pin counts greater than n on a tester having ~~less~~ fewer than n tester channels comprising the steps of:

providing a testing environment of the circuit package;

grouping package pins into banks based on circuit input and output constraints and on the testing environment of the circuit package;

simulating external testing with reduced pin count to remove any test ~~measures~~ output measurements which are outside of an active bank; and

applying testing patterns to the circuit package from tester having ~~less~~ fewer test channels ~~then~~ than pins on the test package.

2. (Original) The method of claim 1 which includes designing the integrated circuit packages to include boundary scan such that most circuit outputs have their driver and enable signals controlled by scannable boundary latches.

3. (Original) The method of claim 2 wherein most circuit inputs have their receiver data observable in scannable boundary latches and with all circuit signal inputs and outputs which do not have boundary latches being included in a bank that is always connected to tester channels.

4. (Original) The method of claim 1 which includes the step of analyzing the integrated circuit physical design data and logical test data.

5. (Original) The method of claim 4 wherein the grouping of pins includes determining presence of differential I/O to be banked.

6. (Original) The method of claim 5 wherein grouping of pins includes determining presence of voltage references to be banked.

7. (Original) The method of claim 6 wherein grouping of pins includes determining presence of I/O with banking restrictions.

8. (Original) The method of claim 7 which includes determining the multiple banking configurations allowable for the integrated circuit package.

9. (Original) The method of claim 8 which includes selecting a banking configuration for the integrated circuit package that can also be used to apply the external tests to other integrated circuits; and allowing the test of several integrated circuits to share the same

banking configuration and hardware.

10. (Currently Amended) A method for parametric testing of an ASIC having a pin counts greater than n on a tester having ~~less~~ fewer than n tester channels comprising:

analyzing the ASIC physical design data and logical test data determining presence of differential I/O voltage reference I/O and I/O with banking restrictions; and

apply testing patterns to the ASIC from the tester having ~~less~~ fewer test channels ~~then~~ than pins on the ASIC.